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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)	
		075834.00036	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]	Application Number		Filed
	09/324,823		June 2, 1999
on	First Named Inventor		
Signature	Takeshi Ide et al.		
Art			Examiner
Typed or printed name Robert J. Depke	2685		Aung Soe Moe
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated on the attached sheet(s).			
Note: No more than five (5) pages may be provide	d.		
applicant/inventor.	-#	//-/	Signature
assignee of record of the entire Interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	Robert J. Depke Typed or printed name 312-277-2006 Telephone number		
attorney or agent of record. 37,607 Registration number			
attorney or agent acting under 37 CFR 1.34.	11/10/06		
Registration number if acting under 37 CFR 1.34	Date		
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
Total of forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:

09/324,823

Confirmation No.: 2056

Applicant:

Takeshi Ide et al.

Filed:

June 2, 1999

TC/A.U.:

2685

Examiner:

Aung Soe Moe

Docket No.:

075834.00036

Customer No.:

33448

PRE-APPEAL BRIEF REQUEST FOR REVIEW ACCOMPANYING NOTICE OF APPEAL

Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

SIR:

ERRORS IN THE PRIOR REJECTION

Consistent with the Review Requirements for identification of clear errors, Applicants note the following:

- I. The combination of references asserted by the Examiner does not teach or fairly suggest a solid-state imaging device wherein a substrate bias voltage is altered depending upon the type of read-out operation such that the saturation signal quantity in the progressive mode is substantially equal to that in the interlaced mode operation.
- The combination of references asserted by the Examiner does not teach or II. fairly suggest a solid-state imaging device wherein a substrate bias voltage is altered depending upon the type of read-out operation such that the saturation signal quantity in a progressive mode in substantially equal to that in the interlaced mode of operation for a HAD sensor.

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REMARKS

A. The §103(a) Prior Art Rejection of Claims 1-3 is Improper based on the combination of Yamaguchi '921, Suzuki '703 and Suga '980

Applicants note that dependent claims 1-3 each respectively specify a solid-state image sensor, a driving method for a solid-state image sensor, and a camera having a solid-state image sensor wherein the driving system operates in a progressive mode in which all picture element signals are output independently and an interlaced mode wherein signals are superimposed. Each of the independent claims specifies that a bias voltage is applied to the substrate in the progressive mode which is smaller than in the interlaced mode such that the applied bias voltages are applied so that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

The Examiner has recognized that the Yamaguchi reference does not teach or suggest the use of a substrate bias circuit and therefore relies upon the teachings of the Suzuki reference. In acknowledging yet another shortcoming of this initial combination of references, the Examiner recognizes that neither Yamaguchi nor Suzuki indicates that a saturation signal quantity in the progressive mode is preferably substantially equivalent to that in the interlaced mode as claimed. Accordingly, the Examiner then cites to the teachings on the Suga '980 reference and asserts that the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

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Fundamentally, Applicants note that this rejection is entirely inappropriate due to the fact that there is no teaching or suggestion demonstrated by the Examiner to make the proposed combination of references as asserted. It is improper to pick and choose randomly from among a variety of cited references to cobble together an obviousness rejection.

Moreover, Applicants note that the so-called bias voltage control of the Suga reference is not actually a substrate bias control as asserted by the Examiner but rather the bias circuit 35 the changes an overflow drain voltage. (See specifically column 6 at lines 30-35). More specifically, in this reference when an excess electric charge is generated at the photodiode, the charge overflows a potential barrier that is determined by the overflow drain voltage VOFD, element 45 and shown in Figure 11 A. Accordingly, this reference merely describes altering an overflow drain voltage according to a field mode operation and a frame mode operation. A person of ordinary skill in the art would not have been motivated to make the proposed combination of references now asserted by the Examiner. Furthermore, even if it were appropriate to make the proposed combination, the asserted combination of references would not result in Applicants' presently claim subject matter.

At best, the combination would merely provide a solid-state imaging device wherein an overflow drain voltage is altered. The asserted combination would not provide adjustment of a substrate bias voltage such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

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Further confirmation of this fact is found in column 7 of the Suga reference at lines 110. This portion of the cited reference describes the selection of the bias for controlling the overflow drain voltage. The reference merely describes increasing the dynamic range by setting the overflow drain voltage to be in a relatively low-level in the frame mode and to be in a "relatively high level" in the field mode. Accordingly, in addition to the fact that the Suga reference does not describe altering a substrate bias voltage, the reference does not teach or suggest altering a bias voltage such that a saturation signal quantity in two modes of operation is substantially equivalent.

At the very least, for these reasons alone, the asserted rejection is improper and should be withdrawn.

A. The §103(a) Prior Art Rejection of Claims 4-5 is Improper based on the combination of Yamaguchi '921, Suzuki '703 Suga '980 and Lee

Fundamentally, this combination of references is similarly deficient for the same reasons as the rejections described above are improper. At the very least, the combination of Yamaguchi and Suzuki have the deficiencies recognized by the Examiner relating to the lack of any teaching or suggestion regarding the specifically claimed adjustment of the substrate bias voltage. As noted, Suga does not fill this void. The Examiner relies upon the Lee reference only for the pinned photodiode structure and this reference does not provide the requisite teaching or suggestion concerning the noted deficiencies described in detail above concerning adjustment of the substrate bias voltage. Accordingly, this combination of

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references remains deficient and the Examiner has failed to establish the obviousness of claims 4-5

C. The §103(a) Prior Art Rejection of Claims 1-3 Is Improper based on the combination of Chang, Suzuki '703 Suga '980 and Lee

The Chang reference suffers from the same deficiencies as the Yamaguchi reference because by the Examiner's own admission, Chang does not teach or suggest controlling a bias voltage applied to the substrate to be smaller for the progressive mode than in the interlaced mode of operation. In support of these rejections, the Examiner again relies upon Suzuki and Suga but these references are deficient for the reasons noted above. Accordingly, this combination of references to similarly deficient in the rejection should be withdrawn.

Applicants note that the same deficiencies apply to the combination of references applied to the obviousness rejection of claims 4-6.

Respectfully submitted,

Date: ////

Robert J. Depke

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